CLAIMS

What is claimed is:

1. An microcontroller integrated circuit, comprising:

a terminal;

a crystal oscillator circuit coupled to the terminal, the crystal oscillator circuit outputting a first clock signal of a first frequency;

a real time clock that receives the first clock signal;

a processor having a clock input lead; and

a clock multiplier circuit having an input lead and an output lead, the clock multiplier circuit receiving the first clock signal from the crystal oscillator circuit and generating therefrom a second clock signal, the second clock signal having a second frequency that is a multiple of the first frequency, wherein the second clock signal is supplied to the clock input lead of the processor.

2. The microcontroller of Claim 1, wherein the first frequency is 32,768 hertz or 32,768 hertz divided by an integer, and wherein the second frequency is greater than 32,768 hertz.

3. The microcontroller of Claim 1, wherein the clock multiplier circuit includes a frequency locked loop, the frequency locked loop including a digital filter.

4. The microcontroller of Claim 3, wherein the frequency locked loop frequency locks a first signal with respect to a second signal, the frequency locked loop further including a ramp generator, wherein the ramp generator starts a first ramp upon a first edge of the first signal,

and wherein a first digital value indicative of a magnitude of the first ramp is determined upon a first edge of the second signal, and wherein the ramp generator starts a second ramp upon a second edge of the first signal, and wherein a second digital value indicative of a magnitude of the second ramp is determined upon a second edge of the second signal, the first and second digital values being used to generate a third digital value, the third digital value being supplied to the digital filter.

5. The microcontroller of Claim 4, wherein the ramp generator receives a slope control input signal, the slope control input signal at least in part determining a slope of the first ramp and a slope of the second ramp.

6. The microcontroller of Claim 5, wherein the slope control input signal is changed during a frequency locking process wherein the first signal is locked with respect to the second signal.

7. The microcontroller of Claim 6, wherein the slope control input signal is a multi-bit digital signal.

8. The microcontroller of Claim 1, wherein the clock multiplier circuit includes a digital filter.

9. The microcontroller of Claim 1, wherein the multiple can be changed by the processor.

10. The microcontroller of Claim 1, wherein the multiple is an integer that can be changed by the processor.

11. The microcontroller of Claim 1, further comprising:

a second terminal, wherein the second clock signal of the second frequency can be output onto the second terminal.

12. The microcontroller of Claim 1, wherein the clock multiplier circuit includes a control loop, the control loop including an oscillator and a loop divider, the loop divider being a counter that is preset with a preset value, and wherein a phase of the second signal is adjusted with respect to the first signal by changing the preset value.

13. The microcontroller of Claim 12, wherein the control loop further inludes a digital filter.

14. The microcontroller of Claim 1, wherein the microcontroller is part of a battery-powered device, and wherein the first frequency is less than 5 megahertz, and wherein the second frequency is greater than 100 megahertz.

15. The microcontroller of Claim 1, further comprising:

a second terminal, wherein a third clock signal on the second terminal can be supplied to the clock input lead of the clock multiplier circuit rather than the first clock signal, and such that the second clock signal output by the clock mutliplier circuit is frequency locked to the third clock signal and not to the first signal, and wherein which of the first clock signal and the second clock signal is supplied to the input lead of the clock multiplier circuit can be changed by the processor.